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A FPGA Implementation based on BIST Architecture for Multiplier Design

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ABSTRACT:Recent strides in programmable logic density, speed and hardware description language (HDL) have empowered the engineer with the ability to implement high-performance digital functionality within the field programmable gate array (FPGA). The ever increasing applications of integrated circuits in the day-to-day useful electronic gadgets is the driving force for the development of low power designs of configurable hardware designs. High speed and low power are the main parameters that are targeted by modern circuit designers. Another important feature of hardware designs is self-testing ability. Considering the architecture on Built-In-Self-Test(BIST) which is low cost and lower time consuming comparing to the Automated Test Equipment (ATE). For BIST, the Test Pattern Generator (TPG) involves with the generation of random number that employs the Circuit Under Test (CUT). This rotational feedback shift register (RFSR) has the characteristics of high speed, low power consumption for TPG and it is especially suited in processing environment where uniform distribution random numbers are required, which is the unique parameter for selecting a random generator sequence. Considering Bit Swapping - Multi Pre-Charged Cyclic Shift Register (BS-MPCCSR) for the reduction of power and delay requirements for the TPG sequence. Also then the out coming stream of bits processes through CUT which here is a multiplier. Then, the response is compared with the signature analyzer. The process of signature analyzer comes with the comparison of test circuit and reference circuit. the outcome of the signature analyzer is Rotational Feedback Shift Register (RFSR) for considering the failure outcomes of the test circuit which is deployed with the chances of using the XNOR instead of XOR logic. That will decrease number of chances of failure outcomes. This feature will gives an improved test sequence for the overall BIST architecture. Thus, by considering the reduction of slices proceeds to the reduction in area, power and delay parameters.

KEYWORDS:Built-In-Self-Test, Test Pattern Generator, Linear Feedback Shift Register, Xilinx, VHDL, Bit Swapping - Multi Pre-charged Cyclic Shift Register (BS-MPCCSR), Rotational Feedback Shift Register (RFSR)
Text detection, Inpainting, Morphological operations, Connected component labelling.

I. INTRODUCTION

Nowadays, the performance of the hardware design can be evaluated using its operational speed and power consumed by the hardware. Field Programmable Gate Array (FPGA) is desired and promising high speed and low power consumption hardware. In FPGA the operation is based on the switching of the internal recourse architecture. For a development of the design, this FPGA can be used and verify the operation of the circuit architecture. If there are any modifications to be done, then we can change the circuit design and again we can verify. Low power system offers benefits like long battery life, high performance, etc. For modern digital applications, high-speed processor with low power consumption design is required. The most common and important module used in the digital signal processors is a multiplier. The multiplier is used to process the complex data. The self testing feature is another feature that is required for testing or diagnosis of the different multiplier architecture. This feature helps the configurable integrated circuits to test by it. In the self-test operation, the hardware is tested by applying different inputs for the functionality of the module. Today's requirement is low power circuit implementation of BIST Based logic circuits on FPGA to achieve high-speed operational circuits. The Test pattern is designed using a modified architecture by reducing the number of sequential circuits.

II. RELATED WORK

[1] proposes on the multipliers that provides in health care sector, most of the calculations are performed that are a important part. [2] In initial test screening process, subtle failures often grow over time, and a substantial fraction of their population can escape. e.g., aging and temperature-drift defects. The temperature-drift test, bring unnecessary power consumption and performance loss, these defects formation over time. Due to the unpredictability of aging failure, conventional tests for aging detection were periodically performed. In low voltage applications, BIST is activated less frequently than in high voltage implementation. Activating BIST too frequently causes a large number of unnecessary chip accesses, which results in large energy consumption BIST generally combines with built-in self-repair (BISR) to improve chip yield. For the designs like SoC and NOC, memory occupies a large area, if there is a small area of defect in founded in the design, the total areas of Soc design gets affected. For avoiding that cases, Built-In-Self- Repair (BISR) logic is used in [3] which combines with the proposed counting threshold algorithm for the BISR scheme that was calculated with the BIST scheme. Considering the test pattern generation the power consumption becomes a more consumable and lesser performance while generating the sequence. In [4], a method is introduced in the research which is focused on LFSR that deals with reduced power consumption and delay. To further reduce with the power consumption, Bit Swapping-Linear Feedback Shift Register. To increase the performance of the circuits Pre-charge technique is used that reduces the delay that improves the maximum switching frequency. Contrary to that above, the BIST scheme, the test pattern generator has the very much vital role in defining the contributions of the transition sequences which is proposed in [5]. Where the test generator method consists of the Multiple Single Input Change vectors. That generates the minimal transition sequence of test patterns. [6] Proposes the work determines the accuracy in extracting the model parameters by considering both random and systematic errors. The random errors are due to the availability of samples (failed SRAM cells). Clearly, more data provides more accurate model parameter extraction.[7]

propose with the embedded BIST scheme that automatically read-disturb fault detection for the development of M-RAM(Magneto Resistive Random Access Memory) which could provide for the enhance in terms of speed and lesser power and higher improved performance that corporate with the Design- for-Testability that utilizes the bit cell test using BIST technique in the health monitoring applications. While dealing with the pattern address generators that should have low transition. So in [8] the method that proposes the address generator that uses the gray code generator with a bit reversal block that has cut down a switch in activity considerably that leads to the reduction in dynamic power consumption. For the testability of the architecture a multiplexer is introduced and proposed in [9]. Whereas in [10], in BIST architecture, the unspecified bits are randomly filled by LFSR reseeding-based test compression scheme, which produces enormous switching activities during circuit testing, thereby causing high test power consumption for scan design. So that, decrease logic transitions in scan chains and reduce specified bit in test cubes generated via LFSR reseeding.

From the above works, the proposed architecture is deals with the Multi Pre-Charged Cyclic Shift Register (BS-MPCCSR)for the reduction of power and delay requirements for the TPG sequence Also then the out coming stream of bits processes through CUT which here is a multiplier. Then, the response is compared with the signature analyzer. The process of signature analyzer comes with the comparison of test circuit and reference circuit. the outcome of the signature analyzer is Rotational Feedback Shift Register(RFSR).

III. PROPOSED SYSTEM

Considering the architecture on Built-In-Self-Test(BIST) which is low cost and lower time consuming comparing to the Automated Test Equipment (ATE). For BIST, the Test Pattern Generator (TPG) involves with the generation of random number that employs the Circuit Under Test (CUT). This rotational feedback shift register (RFSR) has the characteristics of high speed, low power consumption for TPG and it is especially suited in processing environment where uniform distribution random numbers are required, which is the unique parameter for selecting a random generator sequence. Considering Bit Swapping - Multi Pre-Charged Cyclic Shift Register (BS-MPCCSR)for the reduction of power and delay requirements for the TPG sequence. Also, then the out coming stream of bits processes through CUT which here is a multiplier. Then, the response is compared with the signature analyzer. The process of signature analyzer comes with the comparison of test circuit and reference circuit. the outcome of the signature analyzer is Rotational Feedback Shift Register(RFSR) for considering the failure outcomes of the test circuit which is deployed with the chances of using the XNOR instead of XOR logic.

IV. SIGNATURE ANALYZER

If RFSR are used for response analysis then the hardware requirement is very large. A MISR reduces the hardware by compressing the multiple bit streams. Therefore a MISR is used instead of using multiple parallel RFSRs. We can synchronize the Test patterns for BIST with RFSR by using a common clock pulse. The outputs of the CUT are then correlated with an expected patterns response which is also called golden signature. Signature analysis is efficient and widely used compaction technique. MISR compacts all outputs in a single RFSR. RFSR is linear, Also it complies with superposition principle. Its output creates a signature depending on the action of all the bits fed into it. If any bits are wrong or different, the signature will be distinct from the expected value and a fault will have been detected. Only drawback of MISR is that they are susceptible to signature error cancellation and aliasing.

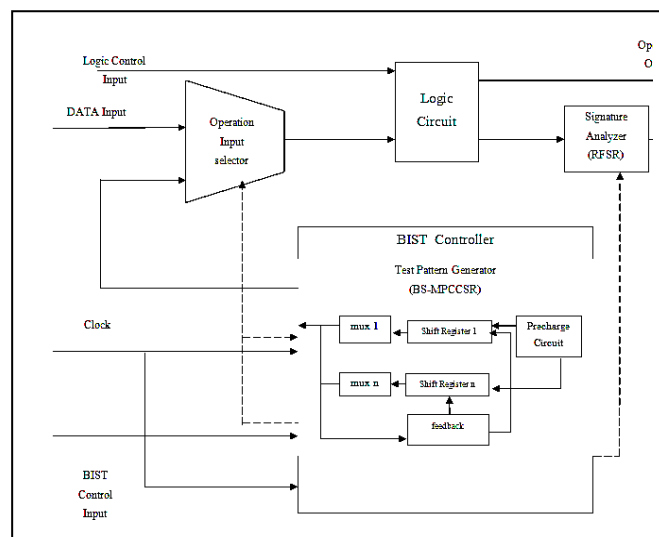


Fig. 1 Architecture of proposed design

V. BIST CONTROLLER

Built-in Self-Test, or BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functional, parametrically, or both) using their own circuits, thereby reducing dependence on an external automated test equipment (ATE). BIST is a Design-for-Testability (DFT) technique, because it makes the electrical testing of a chip easier, faster, more efficient, and less costly. The concept of BIST is applicable to just about any kind of circuit, so its implementation can vary as widely as the product diversity that it caters to. LBIST, which is designed for testing random logic, typically employs a pseudo-random pattern generator (PRPG) to generate input patterns that are applied to the device's internal scan chain, and a multiple input signature register (MISR) for obtaining the response of the device to these test input patterns. An incorrect MISR output indicates a defect in the device. MBIST, as its name implies, is used specifically for testing memories. It typically consists of test circuits that apply, read, and compare test patterns designed to expose defects in the memory device. There now exists a variety of industry-standard MBIST algorithms, such as the "March" algorithm, the checkerboard algorithm, and the varied pattern background algorithm.

BIST control unit regulates and supervises the test execution operation; it supervises the TPG, CUT, TRA and configures the CUT. It is turn on by the normal/test signal. Input MUX is used to switch from normal operating mode to testing mode. In testing mode input vectors are provided by the LFSR. Thus, it controls whether the input is from user or RFSR.

VI. TEST PATTERN GENERATOR

Test pattern Generator creates the test patterns/vectors for CUT. It can be implemented as a standalone circuit. Various techniques for pattern generation, such as deterministic, random or Pseudo random are used. But it is seen that using pseudorandom and random generators results in faster convergence towards a fault. Hence RFSR is used as a TPG. The input of RFSR is a linear function of its preceding state. It is made up of D flip-flops and linear XOR gates. A properly designed RFSR can cycle through $2^n - 1$ unique states. The present work gives the BIST based approach for the implementation of a Vedic multiplier using configurable hardware. A low power 4-bit Vedic multiplier is used to test logic design in the proposed work. The multiplier design is implemented using the gate level architecture representation for realizing low-power hardware. In the RTL schematic of the Vedic multiplier, a gate level combination is used to generate a half-adder and full adder. These designs are used in combination to generate the multiplier using the adder terms. For BIST implantation, test design generators with arbitrary test vectors are required. For TPG design, a Low-power modified design of rotational-feedback-shift register (RFSR) is used. A 3-bit register is used to generate 4-bit random test vectors. It is a comparatively low power design, realization as compared to other existing designs. Most of the TPG has a register-to-bit ratio of 3:4.

VII. EXPERIMENTAL RESULTS

This work simulation and synthesis clearly indicates that the low power implementation, hardware can be used for applications with a configurable IC that has low internal voltage (V_{int}) and low auxiliary voltage (V_{aux}). The present design uses a modified test pattern generator design for BIST implementation. This design can be modified by multiple series combination of similar architecture of logic circuit for a long bit sequence generation of random number. In future the multiplier and the test pattern generator can be configured to match the application specific requirement of the design for a BIST based hardware design implementation. The performance analysis of the proposed system is shown below:

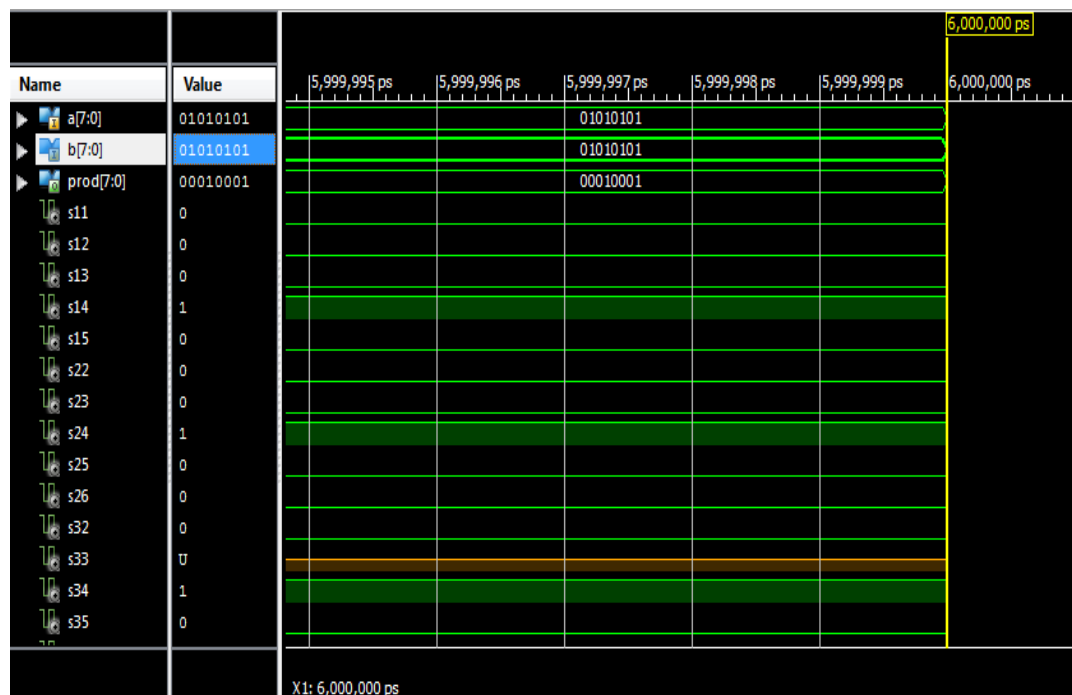


Fig. 2 Performance analysis of BIST architecture

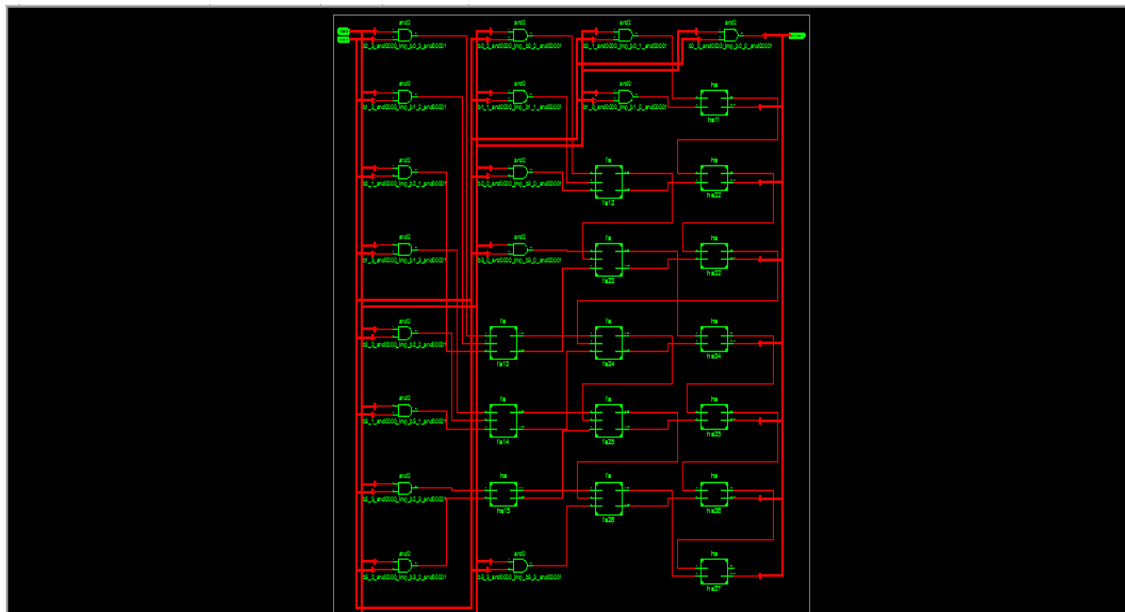


Fig.3 Performance analysis of RTL schematic diagram

VIII. CONCLUSION

In this present work the logic design which is used in the built-in-self-test application is a 4-bit Vedic multiplier and the test pattern generator is also designed for generating random 4-bit vector. Here the test pattern generator has modified to low register-to-bit ratio, i.e. the number of bits sequence generated is more than the number of registers. Thus, the proposed model is very convenient for the users to select the data externally or to generate the data internally to cover all the bits from 0000 to 1111. This work simulation and synthesis clearly indicates that low power is required and high speed performance to develop this application. In future we can use a high speed multiplier rather than Vedic multiplier and also increase the bit sequence by multiple series combination of similar architecture of logic circuit for a long bit sequence generation of random number. For BIST, the Test Pattern Generator (TPG) involves with the generation of random number that employs the Circuit Under Test (CUT). This rotational feedback shift register (RFSR) has the characteristics of high speed, low power consumption for TPG and it is especially suited in processing environment where uniform distribution random numbers are required, which is the unique parameter for selecting a random generator sequence. Considering Bit Swapping - Multi Pre-Charged Cyclic Shift Register (BS-MPCCSR) for the reduction of power and delay requirements for the TPG sequence. Also then the out coming stream of bits processes through CUT which here is a multiplier.

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